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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/635,006	08/06/2003	Koichi Fukuda	OKI.561	7606

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EXAMINER	
HU, SHOUXIANG	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 03/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/635,006	FUKUDA, KOICHI	
	Examiner	Art Unit	
	Shouxiang Hu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 13-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 13-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/28/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Pending claims

According to previous office action, claims 1-6 and 13-20 are pending in this application, and remain active in this Office action.

Claim Objections

Claims 1-6 and 13-20 are objected to because of the following informalities and/or defects:

Claims 1 and 13 each recites the subject matters of "impurity diffused source/drain region," but they each fails to clarify that the source/drain region of the instant invention apparently are formed through implantation (see Figs. 6D and 7A, wherein the source/drain regions are self-aligned with the gate electrode 40, a typical characteristic of the implantation), instead of through diffusion. It is inappropriate to define an implanted region as a diffused region.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5, 13-17, 19 and 20, as being best understood in view of the claim objections above, are rejected under 35 U.S.C. 102(b) as being anticipated by Wakahara (JP 2000-183355; 06/30/2000; of record).

Wakahara discloses an SOI-MOS transistor (Fig. 11) which is naturally capable of functioning as a full depletion type as the SOI layer (3) therein can be as thin as 50 nm (see Paragraph 0020), comprising: a substrate (1); a BOX layer (2); the SOI layer (3) including a channel region and an impurity-doped source/drain region (9); an (element) isolation layer (4) siding the SOI layer on both of the two sides; a gate insulation layer (5); a gate electrode (6); a sidewall (11); and, a high mobility conductive layer including a deposited silicon layer (13b; see Paragraph 0029) underlying a silicide layer (15), wherein the high mobility conductive layer is on and/or extends to the impurity-doped source/drain region, the isolation layer (4) and the sidewall (11), and adjacent to the gate electrode (6). It is noted that the deposited silicon layer (13b) therein is naturally a polysilicon since the nature of the deposition in which at least a portion of the silicon layer (13b) is deposited on the isolation layer (4; silicon oxide); and, wherein the impurity-doped source/drain region and the deposited silicon layer (naturally a polysilicon) together naturally constitute a source/drain of the SOI-MOS transistor (naturally a fully depleted one), since the two are in direct contact with each other.

Furthermore, the device of Wakahara is formed with major process steps that are substantially the same as that of the instant invention. And, in case there is any remaining difference between the two in the details of the process that may be

implicated in the claimed invention, these implicated limitations are process limitations; and these implicated process limitations would not carry patentable weight in this claim drawing to a structure, because distinct structure is not necessarily produced. In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985).

Regarding claims 5 and 17, it is noted that thin silicon layer (3) in Wakahara is naturally about 20 to 80 percent of a total thickness of the polysilicon layer (13b) and the silicide layer (15), as shown in Figs. 10 and 11).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6 and 18, as being best understood in view of the claim objections above, are rejected under 35 U.S.C. 103(a) as being unpatentable over Wakahara in view of Cheng (US 2002/0171107).

The disclosure of Wakahara is discussed as applied to claims 1-5, 13-17, 19 and 20 above.

Although Wakahara does not expressly disclose that the thickness of the SOI layer (thin silicon layer) can be as thin as about 30 nm or less, it is art known that such thickness is well within the commonly recognized range for fully depletion type SOI layer

for achieving desired good channel performance, as readily evidenced in the prior art such as Cheng (see Paragraph 0014).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to SOI device of Wakahara with the thickness of the SOI layer being less than about 30 nm, per the teachings of Cheng, so that a full depletion SOI-MOS transistor with desired good channel performance would be obtained.

Response to Arguments

Applicant's arguments filed on December 28, 2005 have been fully considered but they are not persuasive.

Applicant's main arguments include: the silicon layer 13b in Wakahara is not a deposited polysilicon layer. In response, as explained in the claim rejections above, the silicon layer (13b) in Wakahara is readable as a deposited polysilicon layer, because: (A) it is indeed formed through depositing (see Paragraph 0029); and (B) it is naturally a polysilicon, instead of single crystalline silicon, as at least a portion of the silicon layer (13b) is directly deposited on the isolation layer (4; silicon oxide). Since silicon oxide is naturally amorphous, it lacks regular lattice structure to support and guide the growth of another regular lattice structure on it. Accordingly, at least the portion of the silicon layer (13b) that is directly on the isolation layer (4) is inherently a non-single crystalline one. Thus, the silicon layer (13b) of Wakahara is overall inherently a deposited polycrystalline layer.

In addition, it is noted that the source/drain region of the instant invention is not exactly an impurity-diffusion layer. Instead, it is an impurity implanted one. Furthermore, any implicated process limitation(s) in the claim would not carry patentable weight in this claim drawing to a structure, because distinct structure is not necessarily produced. In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985). In this case, each of the above identified elements of Wakahara has a structure and a material that are both substantially the same as the respective ones recited in the claims of the instant invention, regardless whether there is any differences in the processes of the two.

Furthermore, in response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "condensing does not occur," and "with high reliability") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is 571-272-1654. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SH
March 1, 2006

SHOUXIANG HU
PRIMARY EXAMINER